Claims

What is claimed is:

1. A semiconductor device, comprising:

an integrated circuit die, the integrated circuit die being formed such that at least a portion of at least one perimeter edge of the die is beveled by an etching process.

2. The device of claim 1, wherein the etching process comprises at least one of wet etching and reactive ion etching.

3. The device of claim 2, wherein the wet etching comprises anisotropic etching.

4. The device of claim 1, wherein the at least a portion of the at least one perimeter edge of the integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the device.

5. The device of claim 1, wherein an angle of the beveled portion of the at least one perimeter edge of the integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process.

6. The device of claim 5, wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching.

7. The device of claim 1, further comprising a plurality of integrated circuit die, at least one of the integrated circuit die being separated from the semiconductor device by: (i) forming one or more v-shaped grooves in an upper surface of the device, the v-shaped grooves defining perimeter edges of the at least one integrated circuit die; and (ii) removing a back surface of the semiconductor device opposite the upper surface of the device until at least a portion of the v-grooves are exposed;

wherein a sidewall of each of the v-shaped grooves forms a beveled perimeter edge of the separated die.

8. The device of claim 1, wherein the integrated circuit die is beveled at one or more corners of the die.

9. The device of claim 8, wherein all corners of the integrated circuit die are beveled.

10. The device of claim 8, wherein at least two corners of the integrated circuit die are beveled, an angle of each of the beveled corners being substantially matched to one another.

11. The device of claim 1, wherein an angle of at least one beveled edge of the integrated circuit die is substantially matched to an angle of a sidewall of a die collet configurable for receiving the die.

12. The device of claim 1, wherein at least two perimeter edges of the integrated circuit die are beveled by the etching process.

13. The device of claim 1, wherein all perimeter edges of the integrated circuit die are beveled by the etching process.

14. A method for separating at least one integrated circuit die from an associated semiconductor wafer, the method comprising the steps of:

forming one or more v-shaped grooves in an upper surface of the semiconductor wafer by an etching process, the one or more v-shaped grooves defining perimeter edges of the at least one integrated circuit die; and

removing a back surface of the semiconductor wafer opposite the upper surface of the wafer until at least a portion of the one or more v-shaped grooves are exposed;

wherein a sidewall of each of the one or more v-grooves forms a beveled perimeter edge of the separated at least one integrated circuit die.

15. The method of claim 14, wherein the etching process comprises anisotropic etching.

16. The method of claim 14, further comprising the step of controlling an angle of the sidewall of at least one of the v-shaped grooves, at least in part, by selectively varying one or more characteristics of the etching process.

17. The method of claim 14, wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching.

18. A method for reducing post-fabrication surface damage to an integrated circuit die, the method comprising the step of beveling at least a portion of at least one perimeter edge of the die by an etching process.

19. The method of claim 18, further comprising the step of controlling an angle at which the at least a portion of at least one perimeter edge of the die is beveled by selectively varying one or more characteristics of the etching process.

20. The method of claim 18, wherein the step of beveling comprises forming one or more v-shaped grooves in an upper surface of the integrated circuit die.

21. The method of claim 18, wherein the step of beveling comprises the step of substantially matching an angle at which the at least a portion of at least one perimeter edge of the integrated circuit die is beveled to an angle of at least one sidewall of a die collet configurable for receiving the die.

22. A packaged integrated circuit device, comprising:

at least one integrated circuit die, the at least one integrated circuit die being formed such that at least a portion of at least one perimeter edge of the at least one integrated circuit die is beveled by an etching process.

23. The device of claim 22, wherein the at least a portion of the at least one perimeter edge of the at least one integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the at least one integrated circuit die.

24. The device of claim 22, wherein an angle of the beveled portion of the at least one perimeter edge of the at least one integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process.